IN THE SPECIFICATION:

Please amend the paragraph beginning on page 21, line 18, as follows:

-- The ~~cash~~ cache data column 125 is composed of 32 lines each of which corresponds to a different one of the access unit regions and stores cache data that is a copy of data retained in an access unit region into a corresponding cache line. For each piece of cache data, the logical page address column 121 stores a logical page address that is to be specified when accessing the cache data. The valid bit column 122 stores information showing whether the cache data is valid or not. The dirty bit column 123 stores information showing whether the cache data has been modified from its initial contents. The cache access frequency index column 124 stores an index indicating the frequency of accesses made to the cache data. --

Please amend the paragraph beginning on page 26, line 7, as follows:

-- If the ~~cash~~ cache access frequency index [N, M] is greater than the access frequency index [L], the control circuit 11 updates the access frequency index [L] with the cache access frequency index [N, M] (S133-S134). --

Please amend the paragraph beginning on page 37, line 24, as follows:

-- FIG. 12 is a PAD showing this process. Comparing to the cache flush and TLB update process according to the embodiment 1 (see FIG. 6), the steps S133-S134 of updating an access frequency index based on a cache access frequency index are deleted, while a step S353 of adding ~~A[L]~~ T[L] to an access frequency index is added. Accordingly, an access frequency index in the embodiment 2 indicates a cumulative access count (i.e., a cumulative amount of

degradation having given to the physical page) having been made to a physical page thorough a corresponding logical page. --

Please amend the paragraph beginning on page 55, line 15, as follows:

-- 2) The memory management apparatus according to the embodiment 1 stores, ~~thorough~~ through the cache flush and TLB update process, a peak value of cache access frequency indexes as an access frequency index of a logical page to which cache data belongs, and subsequently invalidates all the pieces of cache data at the same time. --